The Reconfigurable Computing Laboratory at UPR RP

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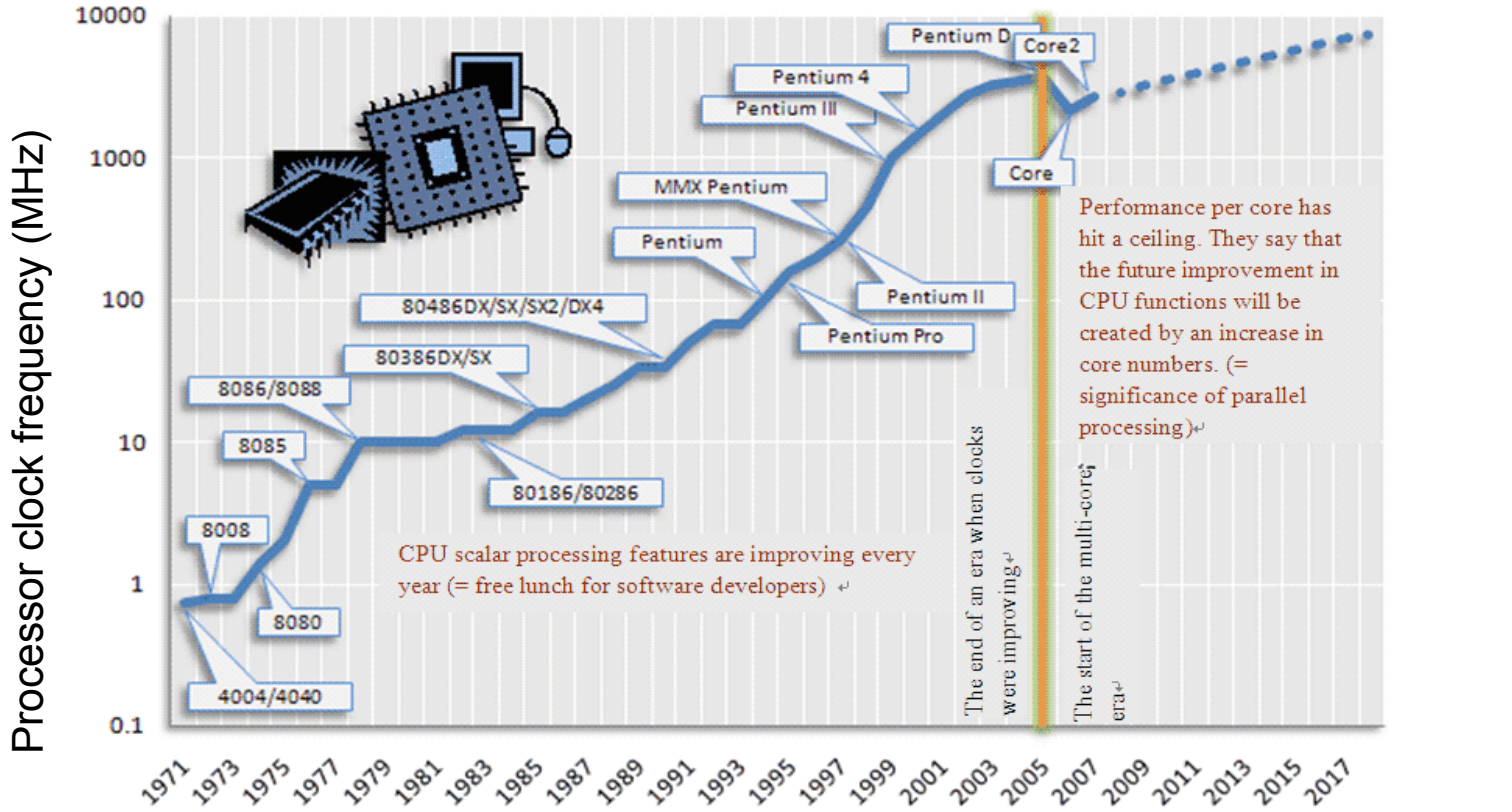
Agenda

- Motivation
- A short story of the rclab@uprrp
- Equipment
- From your idea to to the magic silicon.
- The Mirionics approach
- Project examples

Motivation

- The sequential programming “free lunch is over”



http://numtech.com

- . . . parallelism is here to stay.

Parallelism to the rescue

- Options: take advantage of parallelism in:
  - Distributed, cluster computing.
  - Multi-core General Purpose Processors
  - Graphical Processing Units
  - Reconfigurable Computers

- To the best of our knowledge UPR is only taking (limited) advantage of traditional distributed computing,
- . . and some interesting initiatives in GPUs (UPRH, UPRM) and Reconfig Logic (UPRM, UPR-RP)

FPGAs

- Both of us have had positive research experiences in projects using FPGAs
  - Orozco: Finite field arithmetic units
  - Arce: Eastman Kodak and Dissertation

- Well document history of dramatic speedups and energy efficiency vs. other alternatives.

- Let's make this computing platform technology available to the UPR!
  - A research 'playground' for us.
  - A an educational and production tool for the rest of the university.

NSF-MRI

- *Acquisition of Equipment for the Establishment of a Reconfigurable Computing Center at the UPR*.
  - Requests instrumentation to establish a university center for research, applications and education on Reconfigurable Computing.
  - Instrumentation: Three MVP622 “DUAL QUAD” hybrid computers from Mitrionics AB.
    - Hardware + Development software
    - Added bonus: Open source implementations of usefull applications

NSF-MRI

- Three key activities envisioned for the Center:
  - Support research in diverse areas of knowledge through accelerated applications running on RC's (e.g. BLAST DNA seq alignment, discrete math)
  - Education to create a community of researchers and students knowledgeable and skilled in this powerful computing approach.
  - Research on tools and methodologies to improve design flow from abstraction to implementation on RC.

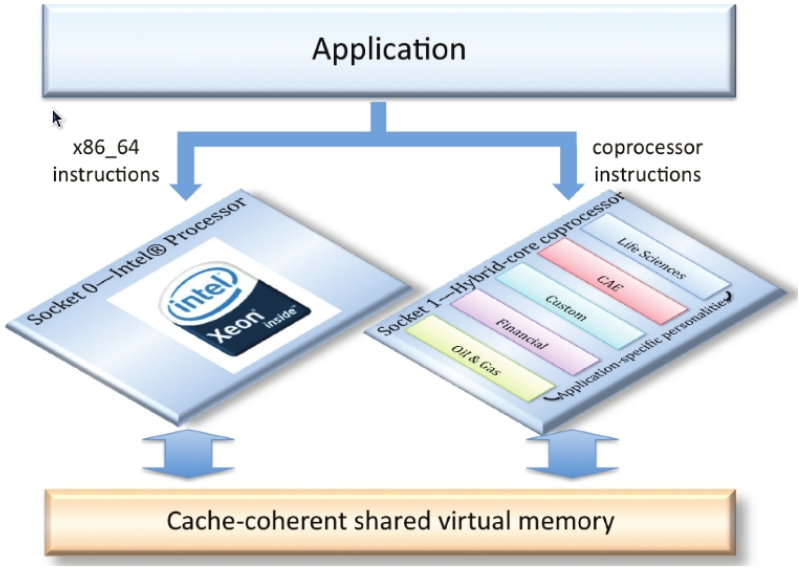
Collaborative Projects

- Hardware/Software Codesign Tools – Arce/Jimenez
- Search for computational results to discrete math problems
  - Latin Square Orthogonality – Rubio/Castro/Cordova/Arce (CS and Math UPR-RP)
  - Hypercube Cut Problem – Emamy (Math)/ Arce
- Fast Finite Field Arithmetic with FPGAs – Orozco/Bollman (UPR-RP/M)
- Reverse Engineering Genetic Networks – Orozco/Bollman/García/Peña (CS UPR-RP/M, Biology UPR-RP)
- Accelerated bioinformatics applications for microbiology – García/Dominguez (Biology UPR-RP)
- Design of Reconfigurable Radar Waveforms – Rodriguez/Jimenez (ECE UPR-M)

Equipment

- 3 Convey HC-1 Servers: each with Intel Dual-core processor + quad-FPGA accelerator.
- Mitrion SDK and MVP licences.

Convey HC-1



The FPGA Co-processor

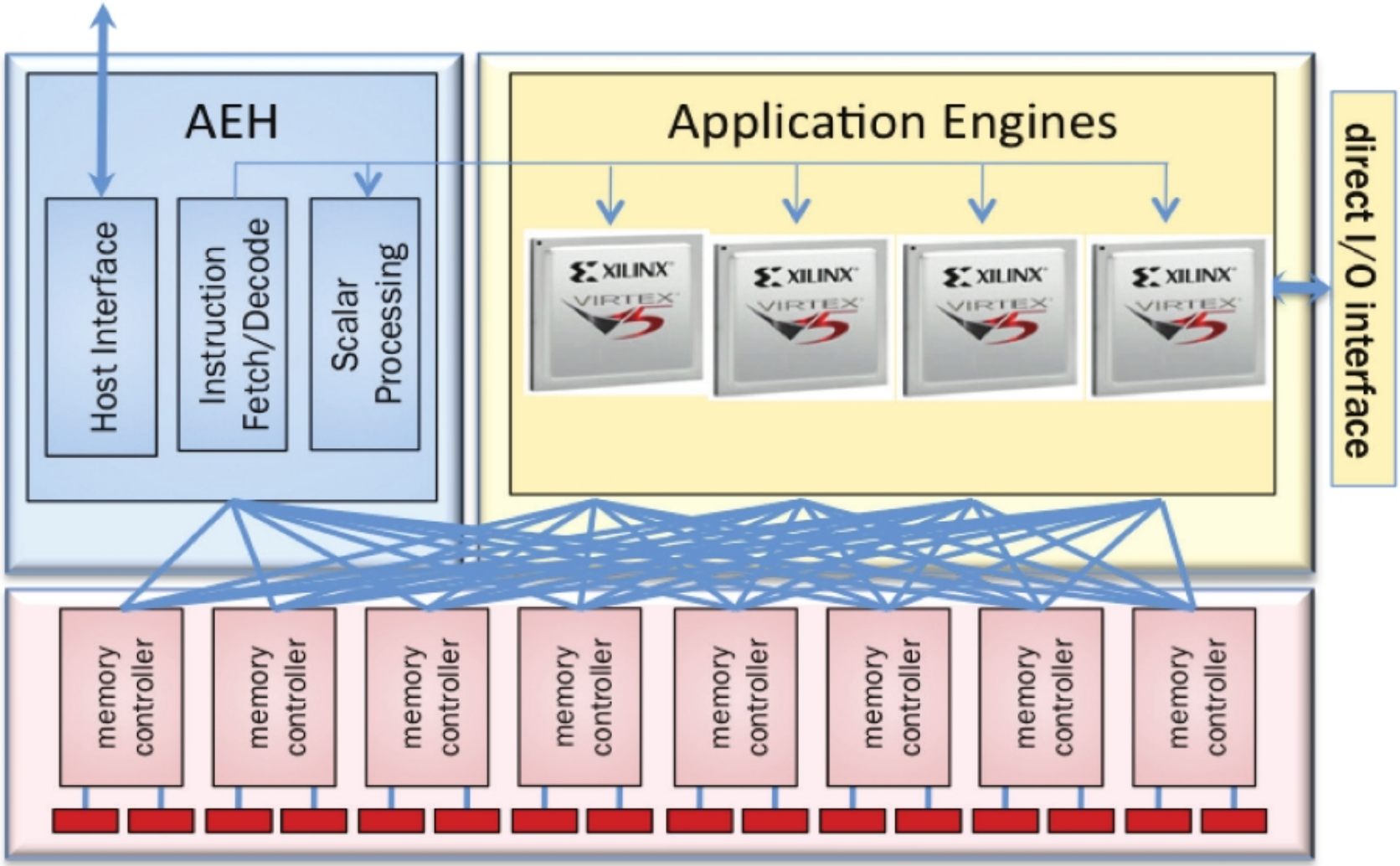


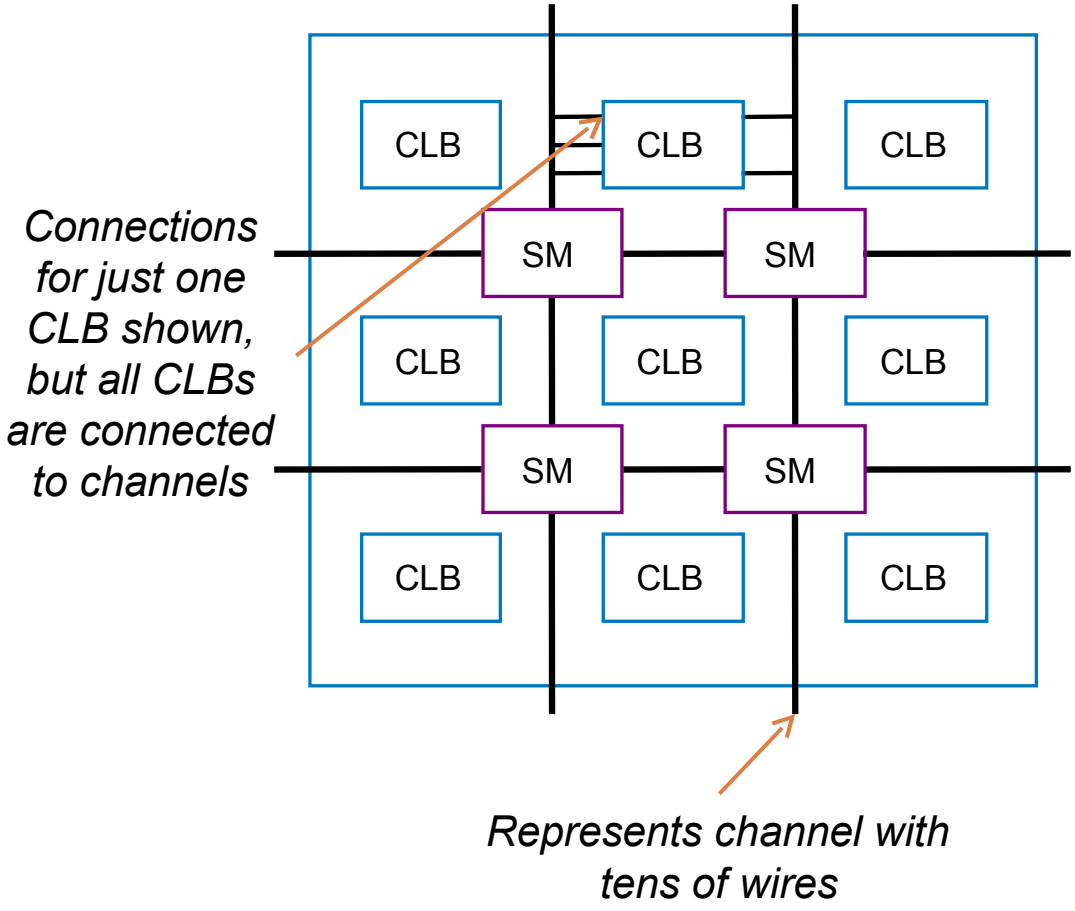
Figure 2. Convey Coprocessor

The FPGA as a coprocessor

- A coprocessor that is customizable to the application.

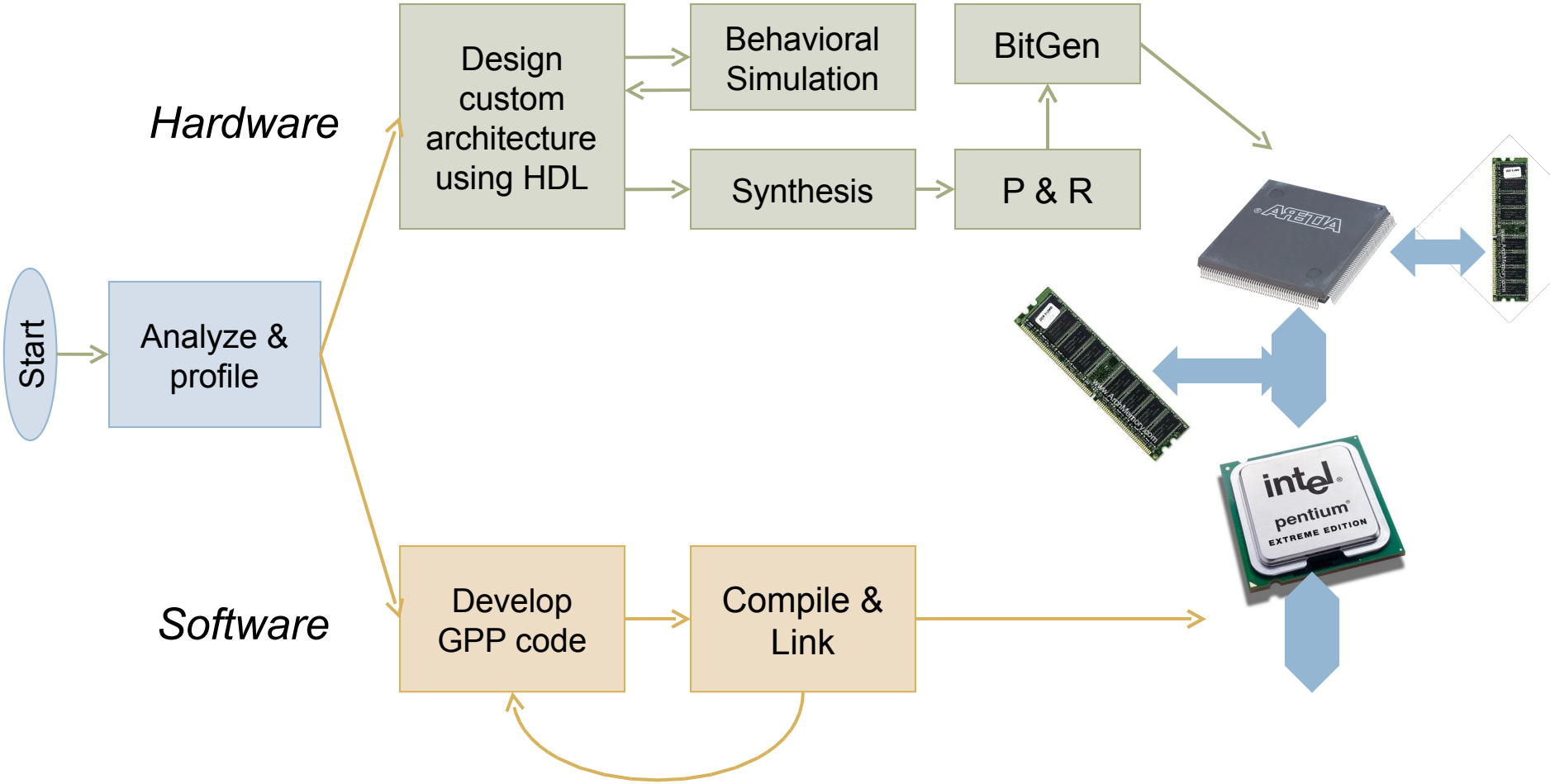
- Finance applications: Random # Gen, MC Simulation
- Digital Signal Processing: FFTs
- Cryptography: Finite field arithmetic

What is an FPGA?

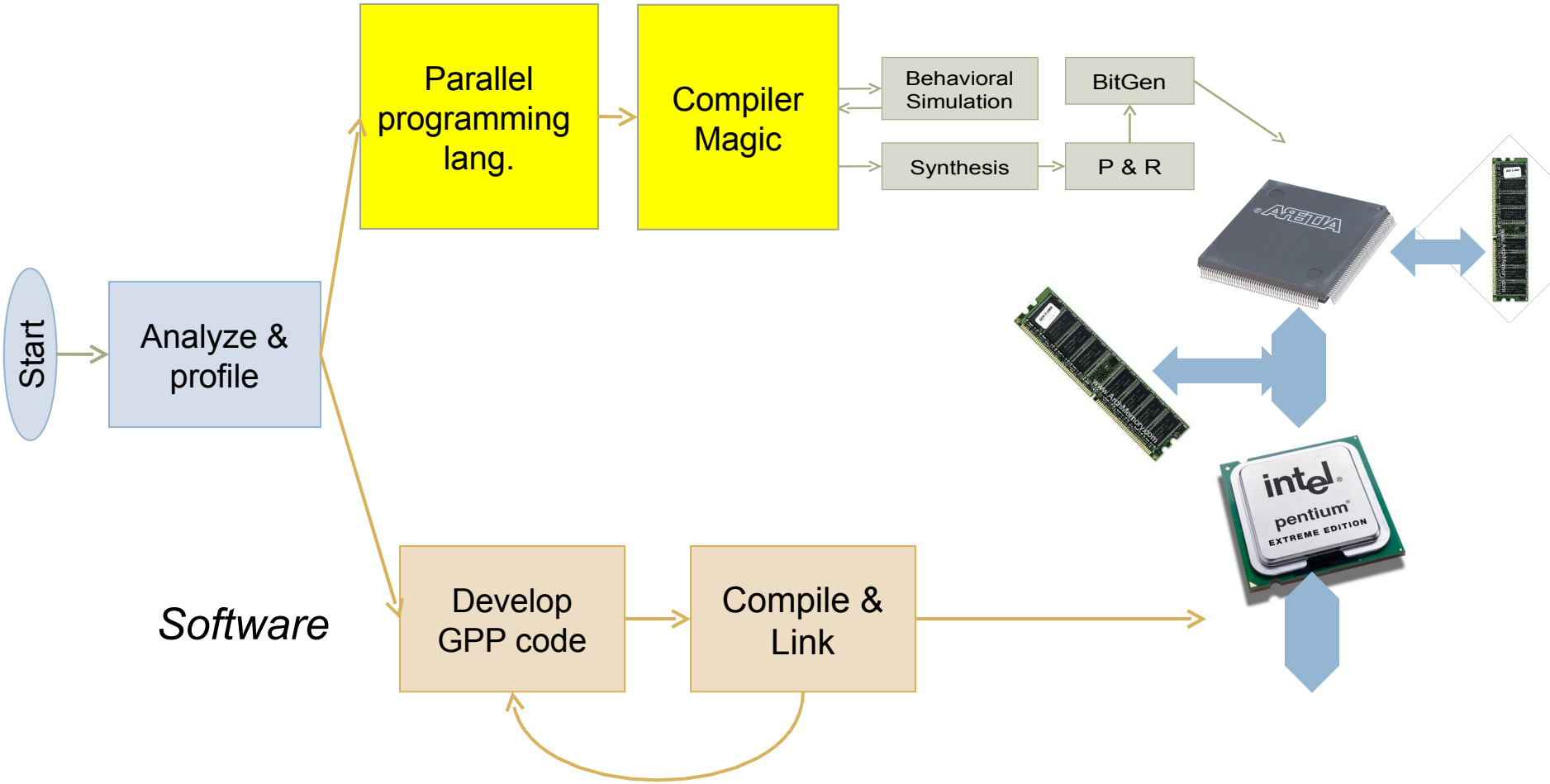


An integrated circuit that consists of an array of (programmable) Configurable Logic Blocks (CLBs) connected by programmable interconnections (switch matrices).

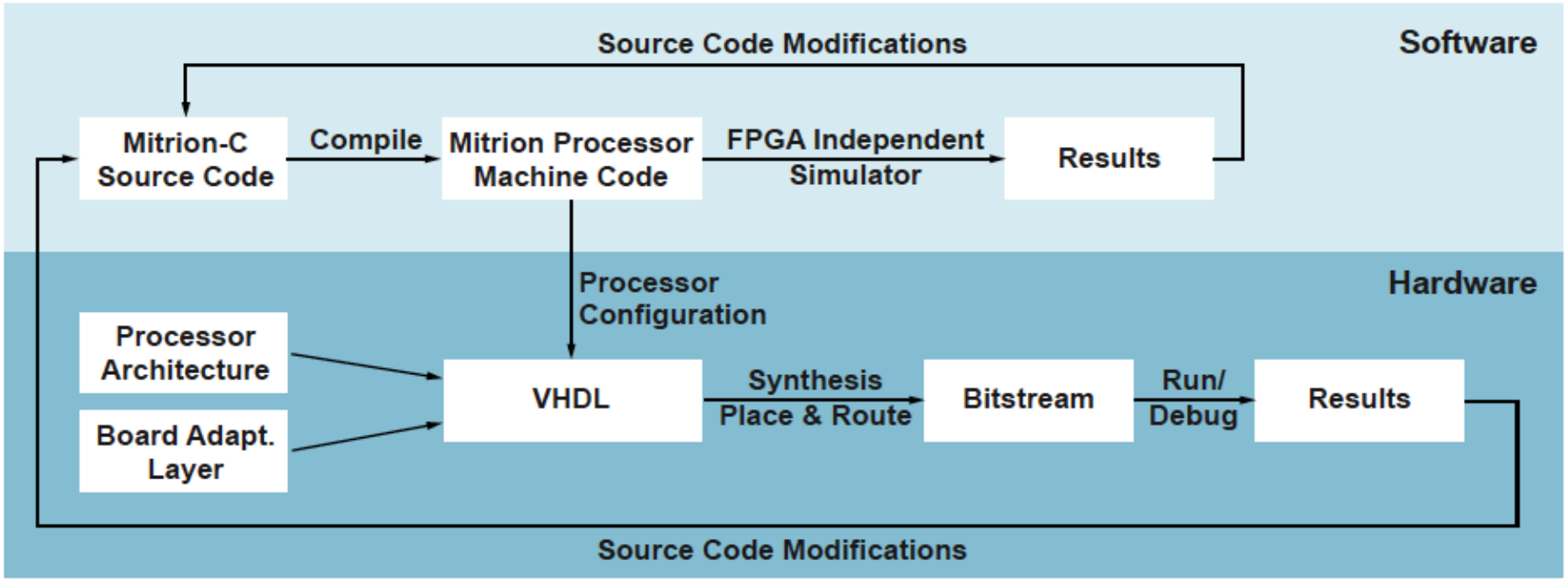
Traditional Hardware/Software Codesign

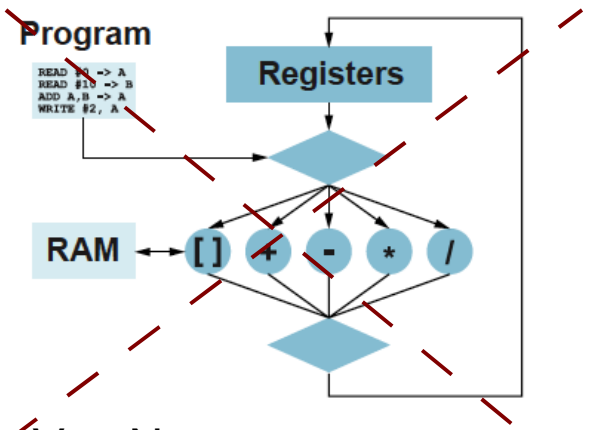


H/S Codesign: Mitrionics Approach

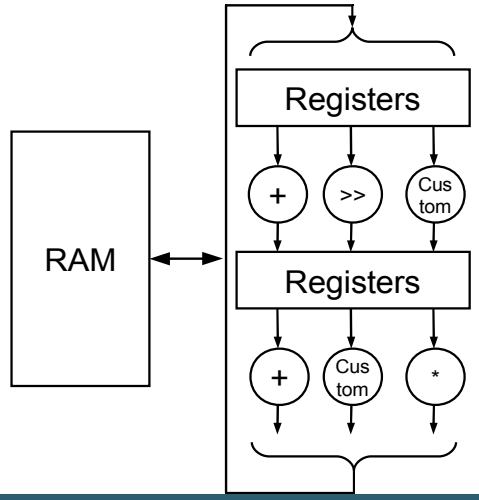


Mitrion C development cycle





Von Neumann processor



Custom
Highly parallelized
Processor

Mitrion C

- The Mitrion-C programming language is an implicitly parallel programming language with syntax very similar to C.
- The main purpose of the Mitrion-C programming language is to aid and support the programmer in fulfilling the requirements of parallel execution.
- In other words, a replacement for HDLs (?)

A taste of Mitrion-C

```
/*************************************************************
 *  Perform matrix multiplication on two matrices
 *  represented as lists.
 */
matmul(matrix_a, matrix_b, ncols)
{
    matrix_c = foreach(row_a in matrix_a)
    {
        FLOAT <ncols> tmp_row_c=foreach(i in < 1..ncols >) (FLOAT) 0.0;
        row_c = for (val_a, row_b in row_a, matrix_b)
        {
            tmp_row_c = foreach(val_b, val_c in row_b, tmp_row_c)
                            val_c + val_b * val_a;
        }
        tmp_row_c;
    }
    row_c;
}
matrix_c;
```

We are in good company

- 3 major research centers have acquire Convey equipment "to explore the application of reconfigurable computing technology to challenging computing problems"
- Lawrence Berkeley Labs:
  - energy-efficient systems to model climate change at unprecedented resolutions
- Stanford University
  - Next gen seismic algorithms, apps to earch sciences
- Oak Ridge National Labs:
  - nuclear energy, climate modeling, open science and other areas supporting the nation's security and infrastructure

We are in good company (cont)

- One of Convey's customers, University of San Diego, has found that they save 90% of power and that they could replace 8 racks of servers with just one rack of Convey servers.

Educational use

- Open invitation to CS and Engineering professors and students who would like to use the RC platform in their courses or research.
- Target courses:
  - Parallel programming
  - Intermediate, advanced digital design courses/labs
  - Hardware description languages
  - Reconfigurable computing / H/S codesign
  - Computer architecture / Hardware arithmetic
  - Special Topics: cryptography, bioinformatics

Educational use

- Main advantages vs. existing FPGA equipment
  - I/O throughput
    - USB (53MB/s) vs. 80GB/s
  - High-end FPGAs!
  - Software Tool Flow
    - Your choice of disparate tools vs. Mitrion
- Advantages over traditional parallel processing
  - Power, space efficiency
  - Higher performance
  - New paradigm

Activities

- Training from Mitrionics
- Training by RCLab and invited personnel
  - Development related
    - Introductory and advanced
  - Production related
    - Sequence Alignment: Mitrion-C Open Bio Project, Smith Waterman
    - Others as requested..
- Training material will be available online through our website: http://ccom.uprrp.edu/~rarce/rclab

A simple example of RC advantage

- Latin square orthogonality

Latin Square Orthogonality

- A latin square of order n is a $n \times n$ array in which each cell contains a single element from an n-set S, such that each element occurs exactly once in each row and exactly once in each column.

$$\begin{pmatrix} 0 & 1 & 2 & 3 \\ 1 & 2 & 3 & 0 \\ 2 & 3 & 0 & 1 \\ 3 & 0 & 1 & 2 \end{pmatrix} \qquad \begin{pmatrix} 2 & 3 & 0 & 1 \\ 0 & 1 & 2 & 3 \\ 3 & 0 & 1 & 2 \\ 1 & 2 & 3 & 0 \end{pmatrix}$$

N	Latin squares of order n
4	576
5	161280
6	812851200
7	61479419904000

- Two Latin Squares are said to be r-orthogonal if when the squares are superimposed we get r distinct order pairs of symbols.

02	13	20	31
10	21	32	03
23	30	01	12
31	02	13	20

Distinct pairs:
{(0,2),(1,3),(2,0),(3,1),
(1,0),(2,1),(3,2),(0,3)
(2,3),(3,0),(1,0),(1,2)}

12-orthogonal

Latin Square Orthogonality

MAIN ROUTINE

```
for every r in R
  for every s in S
    o1 = orto(r,s);
    for every t in S
      Tort = orto(r,s)+orto(r,t)+orto(s,t);
      if Tort > Max_ort then Maxort = Tort;
    next t;
  next s;
next r;
```

```
0 1 2 3 4 5
1 2 3 4 5 0
2 3 4 5 0 1
3 4 5 0 1 2
4 5 0 1 2 3
5 0 1 2 3 4
```

```
0 1 2 3 4 5
3 4 5 0 1 2
4 5 0 1 2 3
1 2 3 4 5 0
2 3 4 5 0 1
5 0 1 2 3 4
```

```
1 0 0 0 0 0
0 1 0 0 0 0
0 0 0 0 0 0
0 0 0 0 0 0
0 0 0 0 0 0
0 0 0 0 0 0
```

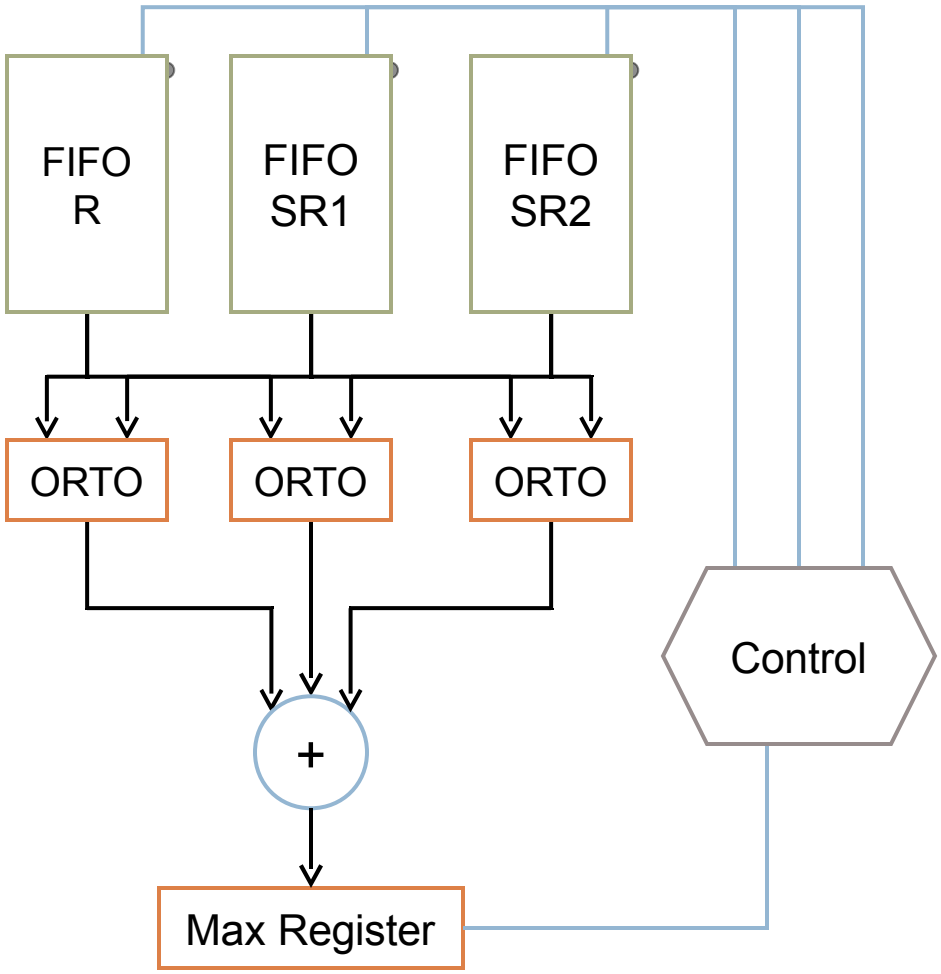
ORTO FUNC

```
function orto(a,b)
  bit pair[6][6] = {0,0,0,..,0}; count = 0;
  for i = 0 to 35
    if pair[a[i],b[i]] = 0 then count++;
    pair[a[i],b[i]] = 1;
  next i;
  return count;
end function orto;
```

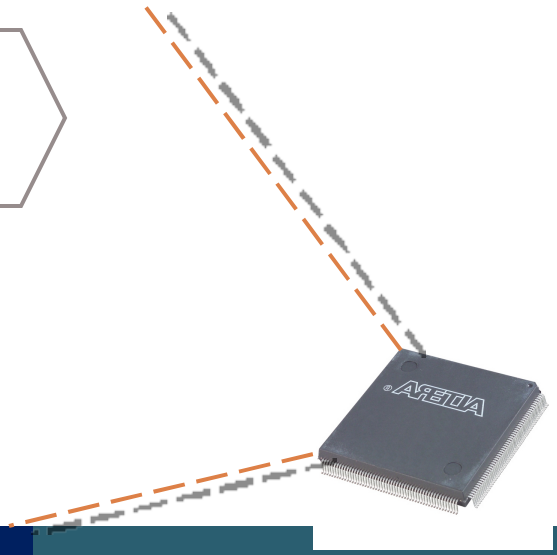
Notice: Accesses to memory, bit manipulation.

Net effect: My PC (2.66GHz Intel Core Duo, 2GB 800MHz RAM) can process 1.45×10^6 LS trios per second.

LS Orthogonality on an RC



- Customized pipeline achieves a 3-orto result per cycle, while registering maximum.
- Running at approximate 150 MHz achieves a ~30x speedup!



Thanks for your attention!

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